Syllabus for ECE 453
Fall 2015
10:10-11:25 T/Th Room Thurston 205
http://apsellab.ece.cornell.edu/ece453/fa15

Discussion:
Th 1:25-2:40pm room Ph314
or
Th 2:55-4:10pm room Ph314
or
W 2:55-4:10pm room Ph 14

Analog Integrated Circuits

Prof. Alyssa Apsel
Phillips 420
Office Hours: Tuesday 3-5pm

TA: Amirmasoud Ohadi <ao328@cornell.edu>, Lab coordinator/Head TA
Location: TBA
Office Hours: Thursday 10am-12pm, 4:15-6:15pm

TA: Mashrur Mohiuddin <mm889@cornell.edu> Homework coordinator
Location: Ph 425
Office Hours: MW 1:30-2:30pm

Course Description: An introduction to Analog Integrated Circuit design for electrical engineering students already familiar with passive circuit analysis and transistor behavior. This course will focus primarily on CMOS analog design and cover material including dynamic circuit analysis, feedback, stability, amplifiers, current mirrors, IC fabrication, and noise analysis culminating in a final design project. Students taking this course are required to have taken ECE 3150 or equivalent. Familiarity with engineering statistics and Laplace/Fourier Transforms is highly recommended.

Prerequisite: ECE 3150 and 2100 or equivalent.

Primary Text:

Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGraw-Hill.

Nice Texts and Papers for Your Enjoyment and Inspiration:

Analog VLSI and Neural Systems, Carver Mead, Addison-Wesley Publishing. Chapter 8.

Analog Integrated Circuit Design, David Johns and Ken Martin, John Wiley & Sons.

Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing, edited by Y. Tsividis and J. Franca.

Low Noise Electronic System Design, C. Motchenbacher and J. Connelly, Wiley.

Policy:

Homework will be assigned roughly once per week and will be given as either a group or individual assignment. Group homeworks are to be completed by assigned groups according to homework policy as stated in class and are to reflect the work of only those named on the turned in assignment. Furthermore, group members not participating in an assignment should not have their names included on the assignment. Assignments will be given in class and are to be turned in at the beginning of class on the due date. Late homeworks will receive a penalty of 20% per day for each late day. Homeworks will not be accepted after 4 days.

Homework Solutions will not be posted. It is your responsibility to make sure you find out how to solve the problems by asking about them in class, during office hours, or in recitation sessions after they have been turned in.

Team homework assignments will include individual effort assignments. The individual assignments will be turned in with the team assignment and will be incorporated into grades. Individuals who do not participate in team assignments may be fired by unanimous consent of the team.

Grading Policy:

The responsibility for grading homeworks will reside with the TA and/or grader. If you believe that a grading error has been made, bring it to the TA during office hours. If you believe that you deserve more points on a given problem, write a statement making your case and deliver it to the TA. Likewise, lab grading questions or complaints should be addressed to the lab coordinator. If you have a question about exam grading, these should be addressed to the course instructor. Grading for this course will be based on the following elements, homework, exams, participation, and project as follows:

10 % Participation – includes in class participation AND seminar attendance when applicable

15 % Homework

15 % Labs

40 % Exams

20 % Final Project

Test Dates:10% Test 1: review material – Oct. 1st, 15% Midterm: ~Oct. 23th,
15% Final: 7pm Dec ?? (as posted)

Expected Background

Upon entering ECE 453, a student is expected to be able to:

Frequency Domain Analysis

- Derive the impulse Response of 1st and 2nd order systems (RC, RLC, LC)
- Derive the step Response of 1st and 2nd order systems (time constants, delay, overdamped, underdamped, critically damped, etc.)
- Construct and read Bode Plots (poles, zeros, magnitude, phase, dB)
- Take Laplace and Fourier transforms

Devices

MOSFETs

- Plot above threshold behavior and recall defining equations
- Label and describe the regions of operation (subthreshold/weak inversion, strong inversion, triode, saturation)
- Describe and Draw small signal models (C_{gs}, C_{gd}, C_{sb}, C_{db}, C_{gb}, g_m, g_{mb}, r_{out}, etc.)
- Explain the physical meanings of all parameters in SSM

BJTs

- Recall and Plot Defining equations
- Label and describe regions of operation from IV curves
- Describe and construct small signal models (C_π, C_μ, C_{cs}, r_b, r_π, r_μ, β, α)
- Explain the physical meanings of each parameter

Use the Miller Approximation to simplify analysis of a circuit

Amplifiers

- For Common Source (describe and plot basic operation, derive input and output impedance, gain, frequency response, and all of the above for cascode configuration, active loads?)
- For Common Gate (describe and plot basic operation, derive input impedance, output impedance, and gain)
- For Common Drain (same as CG)
- For Differential amplifier (same as CG)

At the conclusion of ECE 453, a student will be able to:

Describe the basic operation of a BJT and MOSFET transistor, draw transistor curves for each, write transistor equations for each, and identify regions of operation on transistor curves for each.

Explain the concept of Gm and Rout and how these model parameters relate to transistor curves. Also apply these general concepts to determine gain in more complex circuits such as differential circuits with active loads.

Explain the low frequency behavior of any single stage amplifier, or simple differential amplifier and draw a curve of Vout vs. Vin for CS, CD, CG, and differential amplifier configurations.

Construct a small signal model including parasitic capacitances for any single stage or differential amplifier based on a common source, common drain, or common gate configuration. Use this model to determine gain, input impedance, output impedance, and frequency domain operation of this circuit. Draw Bode plots of circuit behavior as a function of frequency.

Use Miller's theorem to evaluate poles of an amplifier with feedback.

Layout and simulate a circuit using the Cadence design kit. Construct transient responses, DC transfer characteristics, and AC signal analysis. Based upon this data you will be able to verify your hand-calculation analysis and apply these results to a design project.

Differentiate between thermal, shot, and 1/f noise and write expressions for noise in a resistor, diode, or MOS transistor. Explain potential causes for noise in a device.

Derive models for input and output referred noise in amplifiers. Explain noise bandwidth and how it may be calculated or derived as well as how it differs from circuit bandwidth.

Identify feedback within a circuit and explain the class of amplifier (ie. V-V, V-I, I-V, I-I) and type of feedback used. Determine whether feedback is positive or negative.

Identify types of current mirrors and techniques to improve matching and output impedance in a current mirror. Design robust biasing circuits.

List and derive gain and bandwidth expressions for single and 2 stage op-amp designs including folded cascade, telescopic, and active mirror configurations. Be able to determine approximate Bode plots for these amplifiers, headroom limitations, and potential trade-offs for each design. Compare performance of various op-amp topologies and design for given gain and bandwidth requirements.

Describe and evaluate reasons for including common mode feedback as well as methods for doing so including resistive sensing and use of triode MOSFETS.

Evaluate the stability of a system with feedback. Determine phase margin, degree of stability, and construct graphical interpretations of the stability of a system using both Bode plots and root-locus plots.

Design a stable single or two stage amplifier with a given phase margin or stabilize an initially unstable amplifier.