Prefetching using Markov predictors - 25th Anniversary Retrospective

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I. Motivation

Processor performance improvements arise from a combination of process or technology changes, programming model changes to more clearly express parallelism and architectural changes to exploit that ILP. All of these factors come with differing costs and computer architects seek to balance design changes changes to reduce costs. In the 1990's, it was clear that the disparity between CPU and memory speed was an impending issue and microarchitectural techniques such as multi-level caches, varying cache block sizes and cache organizations were important techniques to explore [8]. Later, the "Memory Wall" [19] made clear the disparity between CPU performance and memory speed, both in the instant and the future. Although fundamentally switching the computing model, as called out in the "Memory Wall" paper was possible, there were also opportunities to improve existing architectures through microarchitectural changes.

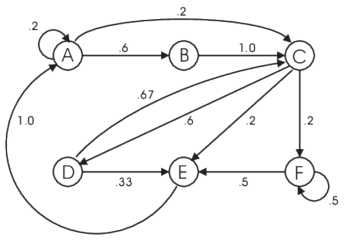
At the time, Doug Joseph was a Ph.D. student at the University of Colorado while also working as a member of the technical staff at IBM working on high performance systems. Dirk Grunwald had been working on improving instruction [11] and data [3] caches. Doug Joseph had an interest an AI and machine learning which is also reflected in his current position on architectural acceleration for deep learning. At the same time, Dirk Grunwald had been working with others on the application of machine-learning to branch prediction using decisions trees [4]. They decided Doug should pursue a thesis based on a preliminary idea that was the gensis of markov prefetching.

At the time, there had been extensive work on memory prefetchers that used arithmetic relations between memory addresses and were effective on structured workloads [6], [10], [13], [15]. Research on prefetching for unstructured workloads was less common [5], [12], [14], [20]. The Markov prefetcher that was the core of Doug Joseph's Ph.D. thesis is a continuing evolution of what has been called *correlation-based prefetching* [1], [5] which was similar to a method patented by Pomerene *et al.* [16].

In correlation prefetching, a memory reference A followed by a miss B would create an entry in a "shadow directory" that recorded that relationship. In [16], the shadow directory was off-chip and the reference stream focused on the miss references from the last-level cache (or references external to the processor). The key idea of Markov prefetching was to extend the simple $A \rightarrow B$ correlation to a full Markov model of prior memory reference behavior.

II. Elaboration

The example from the paper included the following Markov model



constructed from the references **A, B, C, D, C, E, A, C, F, F, E, A, A, B, C, D, E, A, B, C, D, C**. That example highlights most of the challenges that needed to be addressed - the Markov model has nodes with varying out-degree, the predictor could be large, there are both high-predictions and low-probability predictions.

The varying out-degree was addressed by parametric experimentation, but the size of the predictor as well as the number and quality of predictions that were made required more care and, importantly, an analysis method that could simplify performance comparison. There are three important metrics used to compare memory prefetchers: coverage (did you issue a prefetch), accuracy (was it used) and timeliness (did it arrive in time to improve execution). We decided to use a simulation based technique coupled with metrics normalized to the number of demand-references to evaluate different techniques. We used an in-order processor model driven by memory references from scientific and commercial traces that were gathered on an IBM Rs-6000 tracing system. Using whole-system traces was fortuitous – we had previously used whole-program tracing programs like ATOM [18] but that tool couldn't capture O/S interactions and our analysis found that including O/S behavior was very important to understand why we saw improvement in commercial workloads. This allowed us to experiment with different Markov predictor replacement policies and methods to record and then prioritize higher probability prefetch references.

Because the Markov predictor table was quite large (1MByte) an important part of our evaluation was using resource-equivalent predictors to dispel the notion that the large tables were not contributing. For example, we compared a 2MB cache combined with a 1MB predictor table to a 4MB cache organization.

III. Evolution

There were a number of future avenues we wanted to explore. At the time, speculative out-of-order processors were just becoming commercially available with the PentiumPro as the most well-known example. In theory, innovations such as speculative loads coupled with a large number of large miss-status holding registers (MSHR's) could remove some of the near-term miss references. With the introduction of SimpleScalar [2], simulator tooling had improved sufficiently to enable such analysis although without O/S references.

There has been a tremendous amount of innovation in memory prefetching since that the Markov prefecter work. In an effort to address irregular "pointer-chasing" code, Dirk Grunwald worked with another Ph.D. student, Robert Cooksey, on Content-Based prefetching [7] modeled after conservative garbage collection, that prefetches ”likely” virtual addresses observed in memory references. Here the goal was to goal was to capture large portions of the Markov structure using the program data directly.

More recently, machine-learning has been applied to all aspects of computer system design as demonstrated in the ISCA ML architecture systems workshop, including the ML prefetching competition [9]. Systems like Voyager [17] have adopted more sophisticated prediction methods such as LSTM's but also novel methods to reduce the needed state, such as their 2-level prediction structure.

IV. Futures

The memory wall still looms large for computer architecture. At some point, methods like prefetching will reach their achievable limit and alternate architectural mechanisms will be needed, which is why memory-intensive computing has been a ripe area of research and will likely remain so in the coming decades.

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